IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant	: Paul R. Sharps et al.	Art Unit	: 1753
Serial No.	: 10/773,343	Examiner	: Jeffrey T. Barton
Filed	: February 6, 2004	Conf. No.	: 6467
Title	: APPARATUS AND METHOD FOR INTEGRAL BYPASS DIODE IN SOLAR CELLS		

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BRIEF ON APPEAL

(1) Real Party in Interest

The real party in interest is Emcore Corporation, the assignee of the pending application.

(2) Related Appeals and Interferences

The present application is a continuation of U.S. Application No. 10/280,593, which is a continuation-in-part of U.S. Application No. 09/999,598.

An appeal to the Board of Appeals has been filed in connection with U.S. Application No. 10/723,456, which is continuation of U.S. Application No. 09/999,598.

(3) Status of Claims

Claims 38-46, 48-68, 70-73 and 86-111 have been canceled.

Claims 37, 47 and 69 stand rejected and are the subject of this appeal.

(4) Status of Amendments

A final Office action mailed September 20, 2006 rejected claims 37-73 and 86-111. In response to that final Office action, applicants filed, on December 21, 2006, a Request for Continued Examination and a Preliminary Amendment requesting amendments to claims 45-47, 49-50, 52, 86, 90, 92 and 98. The non-final Office action of March 6, 2007 entered those amendments.

An Amendment canceling claims 38-46, 48-68 and 70-111, and re-writing dependent claim 69 in independent form accompanied the Notice of Appeal, filed April 5, 2007, as

permitted under 37 C.F.R. §41.33(b)(2). As indicated by the Advisory action of May 24, 2007, the amendments have been entered.

(5) Summary of Claimed Subject Matter

When solar cells in an array are receiving sunlight or are illuminated, the cells may be forward biased. If some cells in the array are not illuminated, those cells may be forced to become reverse biased in order to carry current generated by other illuminated cells. This reverse biasing can degrade the non-illuminated cells and ultimately render them inoperable. In order to prevent damage to the non-illuminated cells, a diode structure can be implemented in an alternate parallel path that draws away current and maintains a connection to the next cell.

In prior designs, the solar cell and bypass diode were provided as discrete devices. The present application discloses, among other things, an integrated structure which, in some cases, can result in a less expensive design.

Claim 37

Independent claim 37 recites a semiconductor structure that includes a multijunction solar cell having first and second subcells and a bypass device having p-type, i-type and n-type layers. Claim 37 further recites that the bypass device and a subcell integral to the bypass device have an identical sequence of semiconductor layers where each layer in the bypass device has substantially the same composition and thickness as the corresponding layer in the subcell.

Examples are illustrated in FIGS. 6 and 8 of the present application. In the example of FIG. 8, a triple junction solar cell structure 640 is shown that includes bottom, middle, and top subcells 604-608 for converting solar power to electrical power in a portion 642 (*see* ¶ 54, 67 of present application). FIG. 8 also shows a portion 644 to the right of portion 642 which includes (1) a bypass diode 620 having an n-type layer 860, i-type layer 862 and p-type layer 864 and (2) subcells 604-608 over which the bypass diode 620 is formed (*Id.* ¶ 54, 73).

In the illustrated example, the portion 644, which includes bypass diode 620 and subcells 604-608, is integrally connected to the subcells 604-608 of portion 642 through substrate 602. Each layer in the subcells 604-608 of portion 644 has substantially the same composition and thickness as the corresponding layer in the subcells 604-608 of portion 642.

Claim 47

Claim 47 recites a solar cell semiconductor device that includes a sequence of layers of semiconductor material, in which the sequence of layers forms a sequence of cells of a multijunction solar cell in a first region and also forms, in a second region, a support for an integral bypass diode to protect the sequence of cells against reverse biasing at less than breakdown voltage. Claim 47 further recites that the bottom layer of the bypass diode and the top layer of the top cell of the sequence of cells have a first polarity and that the sequence of layers in the second region is laterally separated and laterally spaced apart from the first region.

As shown in the example of FIG. 8, a sequence of layers of semiconductor material forms subcells 604-608 of triple junction solar cell 640 in portion 642 and also forms subcells 604-608 in portion 644 that support bypass diode 620. The layers of subcells 604-608 in portion 642 are laterally spaced apart and laterally separated from the layers of subcells 604-608 in portion 644. In the illustrated example, the top layer 846 of the top subcell 608 and the bottom layer 860 of bypass diode 620 have the same polarity (*i.e.,* n-type) (*Id.* ¶ 71, 73).

Claim 69

Claim 69 recites a solar cell semiconductor device that includes a first sequence of layers of semiconductor material on a substrate, in which the first sequence of layers forms at least one cell of a multijunction solar cell in a first region. A second region includes the first sequence of layers in addition to a second sequence of layers that forms a bypass diode having p-type, n-type and i-type layers. The bottom layer of the bypass diode and the top layer of the top cell of the multijunction solar cell have a first polarity. Claim 69 further recites that a metal layer deposited on the substrate and over a portion of the second region electrically shorts the first sequence of layers of the second region.

An example of the metal layer is the metal shunt 630 (FIG. 8), which is connected to both the substrate 602 and a lateral conduction layer 610 and which "shorts a portion of the multijunction solar cell structure that is underneath the bypass diode 620" (*Id.* ¶ 61, 74 and FIGS. 6, 8). Since the shunt 630 is made of metal, it provides a low resistance pathway for the majority of current to travel from the substrate to the bypass diode 620, instead of mainly through the

layers of subcells 604-608. Accordingly, the voltage necessary to draw current away from non-illuminated solar cells can, in some implementations, be reduced.

(6) Grounds of Rejection to be Reviewed on Appeal

(A) Whether claims 37, 47 and 69 are unpatentable under 35 U.S.C. § 112, first paragraph because of the language "substantially the same composition and thickness."

(B) Whether claim 37 is unpatentable under 35 U.S.C. § 112, first paragraph because of the language reciting "a bypass device . . . having p-type, i-type and n-type layers . . ."

(C) Whether claims 37, 47 and 69 are unpatentable under 35 U.S.C. § 112, second paragraph because of the language "substantially the same composition and thickness."

(D) Whether claim 47 is unpatentable under 35 U.S.C. § 102(b) as anticipated by JP 9-64397 (Fujioka) or WO 99/62125 (Ho et al.).

(E) Whether claim 69 is unpatentable under 35 U.S.C. § 102(b) as anticipated by JP 9-64397 (Fujioka).

(7) Argument

(A) The language "substantially the same composition and thickness" in claims 37, 47 and 69 does not render those claims unpatentable under 35 U.S.C. § 112, First Paragraph

The Office Action alleges that the language "substantially the same composition and thickness" fails to satisfy § 112, ¶ 1 "because there is simply no support for the broadening term 'substantially' in the specification as filed." (Office Action mailed March 6, 2007, p. 17). Applicant respectfully submits that the Examiner has misinterpreted and misapplied the requirements of § 112, ¶ 1.

Although, as disclosed in the specification, the deposited semiconductor layers can generally be characterized as having "the same" composition and thickness, a person of ordinary skill in the art would have understood that the deposition process of the type described in this Application inherently leaves small variations in the thickness and composition of the deposited layers, resulting in layers that are "substantially the same" in thickness and composition. Thus,

out of an abundance of caution and in the interest of technical accuracy, Applicant amended the claims to recite the phrase "substantially the same."

It is well-established that lack of literal support in the specification for claim language is not enough to support a rejection under § 112, ¶ 1. *See, e.g., Eiselstein v.* Frank, 52 F.3d 1035, 1039 (Fed. Cir. 1995); *Kao Corp. v. Unilever U.S., Inc.*, 441 F.3d 963, 968 (Fed. Cir. 2006). As the MPEP states, "the subject matter of the claim need not be described literally (i.e., using the same terms or *in haec verba*) in order for the disclosure to satisfy the description requirement." MPEP § 2163.02.

Instead, the appropriate inquiry under § 112, ¶ 1 is whether the specification "describe[s] an invention in sufficient detail that one skilled in the art can clearly conclude that the inventor invented what is claimed." *Kao Corp.*, 441 F.3d at 967-968. "If a person of ordinary skill in the art would have understood the inventor to be in possession of the claimed at the time of filing, even if every nuance of the claims is not explicitly described in the specification, the adequate written description requirement is met." *In re Alton*, 76 F.3d 1168, 1175 (Fed. Cir. 1996).

Moreover, where, as here, an applicant files a declaration explaining why those skilled in the art would find support in the specification for the claimed subject matter (*see* Applicant's §1.132 Declaration), the examiner cannot dismiss the declaration without "articulating adequate reasons to rebut" the declaration. *In re Alton*, 76 F.3d 1168, 1176 (Fed. Cir. 1996); *see also* MPEP § 716.01(B) ("[T]he examiner must specifically explain why [the declaration] is insufficient. General statements . . . without an explanation supporting [his or her] findings are insufficient.").

In particular, Applicant submitted a declaration under 37 C.F.R. §1.132 demonstrating why the phrase "substantially the same" thickness and composition more accurately covers the compound semiconductor layer and is supported by the specification as would be understood by those skilled in the art. (*See* Applicant's § 1.132 Declaration, p. 3) In view of the declaration submitted by Applicant, it was incumbent upon the Examiner to articulate adequate reasons for dismissing the evidence set forth in the declaration. *Kao Corp.*, 441 at 967-968 (Fed. Cir. 2006); MPEP §716.01(B). The Office action, however, did not articulate any reasons for dismissing the declaration except that the word "substantially" is not *literally* used in the specification to describe the claimed invention. This reason alone is not sufficient to support a rejection under §

112, ¶ 1. *See Eiselstein*, 52 F.3d at 1039; *Kao Corp.*, 441 F.3d at 968. Absent adequate reasons for dismissing Applicant's declaration, the Examiner's rejections under § 112, ¶ 1 are in error. *In re Alton*, 76 F.3d at 1176.

In view of the foregoing, the rejections of claims 37, 47 and 69 – as allegedly failing to satisfy the requirements of section 112, first paragraph because of the language "substantially" the same composition and thickness – should be reversed.

(B) The language of "a bypass device . . . having p-type, i-type and n-type layers . . ." in claim 37 does not render that claim unpatentable under 35 U.S.C. § 112, First Paragraph

The Office Action alleges that claim 37 fails to satisfy § 112, ¶ 1 because "there is no support in the specification as originally filed for a bypass device having p-type, i-type, and n-type layers, wherein the bypass device and a subcell of a multijunction cell have an identical sequence of layers with substantially the same thickness and composition." In particular, the Examiner alleges that the p-type, i-type, and n-type layers 622-626 of bypass diode 620 correspond to the claimed "bypass device" and that there is "no teaching of a p-i-n cell anywhere in the specification as filed" (*see* Office Action mailed March 6, 2007, p. 4). As explained below, that is incorrect.

Although the layers 622-626 form a bypass diode 620, there is nothing in the claim language or in the specification that limits the claimed "bypass device" to include only these layers. Instead, the claimed "bypass device" may include layers in addition to the p-type, i-type, and n-type layers 622-626. For example, the layers of bottom cell, middle cell and top cell 604-608, in portion 644, form a support for the bypass diode 620 (*see* FIG. 6 of present application) and, therefore, also can be considered as *part of* the "bypass device." It follows that each layer in sections 604-608 of the illustrated "bypass device" has "substantially the same composition and thickness" as a corresponding layer in the subcells 604-608 in portion 642 of the solar cell.

Furthermore, contrary to the Examiner's assertion that there "is no teaching of a p-i-n cell anywhere in the specification," FIGS. 6 and 8 and paragraphs 58, 73 of the specification as filed disclose that bypass diode 620 includes p-type, i-type and n-type layers.

In view of the foregoing, it is evident that the specification as filed provides sufficient support for the features recited in pending claim 37 and, therefore, the rejection of claim 37 under section 112, first paragraph should be reversed.

(C) The Rejections of Claims 37, 47 and 69 under 35 U.S.C. § 112, Second Paragraph Should Be Reversed

The Office Action alleges that the phrase "substantially the same thickness and composition" is indefinite under § 112, ¶ 2 because "it is not clear what is to be encompassed by [this] term." (Office Action mailed March 6, 2007, p. 6)

Applicant's position – that the word "substantially" as used in the pending claims satisfies the requirements of § 112, ¶ 2 – is supported by numerous Federal Circuit decisions approving the use of the term "substantially" under § 112, ¶ 2. *See, e.g., Verve*, 311 F.3d 1116, 1119-20 (Fed.Cir. 2002); *Ecolab Inc. v. Envirochem, Inc.*, 264 F.3d 1358, 1367 (Fed.Cir.2001); *Howmedica Osteonics Corp. v. Tranquil Prospects, Ltd.*, 401 F.3d 1367, 1373 (Fed. Cir. 2005); *LNP Engineering Plastics, Inc. v. Miller Waste Mills, Inc.*, 275 F.3d 1347, 1356 (Fed. Cir. 2001); *Andrew Corp. v. Gabriel Electronics, Inc.*, 847 F.2d 819, 821 (Fed. Cir. 1988); *Seattle Box Co., Inc.*, 731 F.2d at 826; *Kinzenbaw v. Case LLC*, 179 Fed.Appx. 20, 30 (Fed. Cir. 2006); *see also* MPEP 2173.05(b).[1] The Federal Circuit also has upheld the definiteness of claim terms that closely resemble "substantially the same," including "substantially equal," "substantially equal to" and "substantially uniform." *See Andrew Corp.*, 847 F.2d at 821 ("substantially equal"); *Seattle Box Co., Inc.*, 731 F.2d at 826 ("substantially equal to"); *Ecolab Inc.*, 264 F.3d at 1367 ("substantially uniform").

Applicant's § 1.132 declaration also supports the conclusion that the phrase "substantially the same composition and thickness" meets the requirements of § 112, ¶ 2. (*See* Applicant's § 1.132 Declaration, ¶ 2-8)

Nevertheless, the Office Action rejects the arguments raised in Applicant's § 1.132 declaration because it allegedly is "not clear how close to having the same thickness the corresponding layers must have in order to be considered to have 'substantially the same

[1] The Federal Circuit, furthermore, has also found definite the term "substantially" even though it did not appear in the specification. *See Ecolab, Inc.*, 264 F.3d at 1367; *LNP Engineering Plastics, Inc.*, 275 F.3d at 1355.

thickness.'" (Office Action mailed March 6, 2007, p. 18) The Office Action further alleges that "the designation of two to three percent variation in a declaration does not render the claim language definite." (*Id.*, p. 18)

Applicant disagrees with the Examiner's conclusions. Contrary to the remarks of the Examiner, the specified normal range of up to two to three percent variations makes clear "how close to having the same thickness the corresponding layer must be" and falls well within manufacturing specifications for actual commercial products. (*See* Applicant's § 1.132 Declaration, p. 2.)

To the extent the Examiner's rejection is based on a perception that the term "substantially" bears some imprecision, Applicant respectfully submits that § 112, ¶ 2 does not impose such a high threshold for claim definiteness. "That some claim language may not be precise . . . does not automatically render a claim invalid." *Seattle Box Co. v. Industrial Crating & Packing*, 731 F.2d 818, 826 (Fed.Cir.1984). The MPEP instructs examiners in a similar vein:

> When the examiner is satisfied that patentable subject matter is disclosed, and it is apparent to the examiner that the claims are directed to such patentable subject matter, he or she should allow claims which define the patentable subject matter with a reasonable degree of particularity and distinctness. Some latitude in the manner of expression and the aptness of terms should be permitted even though the claim language is not as precise as the examiner might desire.

MPEP § 2173.02. Although claims that are "insolubly ambiguous" or "not amendable to construction" are indefinite under § 112, ¶ 2, *Datamize, LLC v. Plumtree Software, Inc.*, 417 F.3d 1342, 1347 (Fed. Cir. 2006), where, as here, "the term 'substantially' serves reasonably to describe the subject matter so that its scope would be understood by persons in the field of the invention, . . . it is not indefinite." *Verve, LLC v. Crane Cams, Inc.*, 311 F.3d at 1120.

For at least the foregoing reasons, Applicant submits that the rejections of claims 37, 47 and 69 under section 112, second paragraph should be reversed.

(D) <u>The Rejection of Claim 47 Under 35 U.S.C. § 102(b) Should Be Reversed</u>

As explained by the MPEP (§ 2131), a claim is anticipated under 35 U.S.C. § 102(b) "only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." As discussed below, that is simply not the case here.

Claim 47 recites a solar cell semiconductor device that includes, among other things, a first region in which a sequence of layers forms a sequence of cells of a multijunction solar cell. In a second region, the same sequence of layers is laterally spaced apart and laterally separated from the first region, and the sequence of layers forms a support for an integral bypass diode to protect the sequence of cells against reverse biasing at less than breakdown voltage.

(i) Claim 47 is patentable over WO 99/62125 (Ho et al.)

As explained below, the Ho et al. reference does not disclose a sequence of layers, in a second region, that "forms a support for an integral bypass diode" and that is "laterally spaced apart and laterally separated" from a first region as recited in claim 47.

The Ho et al. reference discloses a solar cell (*see* layers 1402-1432 on left side of the small trough 1438 in FIG. 14B) connected to a bypass diode 1410 (*see* GaAs Base/Buffer 1412 and GaAs emitter 1414 on right side of the small trough 1438 in FIG. 14B). An AlGaAs window 1416, tunnel diode layers 1418, 1420 and a front metal 1440 are formed on the surface of the bypass diode layers 1412, 1414.

The Examiner alleges (*see* Office Action mailed March 6, 2007, p. 19) that, "at minimum," a Schottky diode formed at the interface between tunnel diode layer 1420 and front metal 1440 corresponds to the claimed "bypass diode." The Examiner further alleges (*Id.*, p. 19) that the GaAs Base/Buffer 1412, GaAs emitter 1414 and AlGaAs window 1416 correspond to the claimed "sequence of layers of semiconductor material" that form "a support" for the bypass "Schottky" diode. Applicant submits that the Examiner's interpretation and application of the reference to the claimed subject matter is incorrect.

First, the GaAs base/buffer layer 1412 and GaAs emitter layer 1414 do not "form a support" for a bypass diode. Instead, those layers *are* the bypass diode. That is consistent with the Ho et al. reference which states, on pg. 8, lines 11-12, that the isolated diode layers 1412-1420 (on the right-hand side of FIG. 14B) "form a portion of the bypass diode *function*." Likewise, FIG. 14B of the Ho et al. reference clearly illustrates that layers 1412 and 1414 are part of bypass diode 1410.

Support for bypass diode 1410 is instead provided by the underlying tunnel diode layers 1408, 1406 and the Ge substrate 1402. Tunnel diode layers 1408, 1406 and Ge substrate 1402 are not, however, "laterally spaced apart and laterally separated" from a first region as recited in pending claim 47 and, therefore, do not correspond to the claimed "sequence of semiconductor layers" that form a support for a bypass diode.

Second, although the layers 1412, 1414 of the bypass diode 1410 (right side of FIG. 14B) are separated from similar layers in the solar cell (left side of FIG. 14B), there is no disclosure in the Ho et al. reference that the layers 1412, 1414 support either a Schottky diode or other diode that corresponds to the claimed bypass diode.

Regarding the existence of a Schottky diode, the Examiner merely asserts that "it is the Examiner's position" the front metal contact 1440 forms a Schottky junction with the tunnel diode layer 1420 (Office Action mailed March 6, 2007, p. 12) without providing any explanation or evidence to support this allegation. Applicant notes that it is well known by those skilled in the art that not all metal-semiconductor junctions necessarily exhibit Schottky diode behavior.

Indeed, it would not make sense to include a Schottky diode at the interface of the metal contact 1440 and tunnel diode 1420 because the presence of a Schottky diode at that interface would raise the turn-on voltage of the bypass diode 1410. Raising the turn-on voltage of the bypass diode 1410 increases the possibility that the photovoltaic portions of solar cell 1400 will reach a breakdown voltage under reverse bias, which can damage the solar cell.

Nor do the tunnel diode layers 1418, 1420 themselves function as a bypass diode when the solar cell 1400 is under forward or reverse bias. Bypass diodes *allow* the flow of current when the solar cell is reversed biased and *block* the flow of current when the solar cell is forward biased. However, under the anti-parallel configuration shown in FIG. 14B of the Ho et al. reference, the tunnel diode layers 1418, 1420 are forward biased and thus *allow* current to flow when the solar cell 1400 is also forward biased. Furthermore, in contrast to the description of a bypass diode disclosed by the Ho et al. reference (p. 1, lines 27-28), the tunnel diode layers 1418, 1420 do not become forward biased when the solar cell is shadowed. Instead, the anti-parallel configuration ensures that layers 1418, 1420 are reverse biased when the solar cell 1400 is

reverse biased. In view of the foregoing, it is clear that the tunnel diode layers do not function as a bypass diode.

Moreover, the tunnel diode layers 1418, 1420 do not correspond to a bypass diode that "protect[s] a sequence of cell against reverse biasing" as recited in claim 47. Instead, as with tunnel diode layers 1406, 1408 (*see* Ho et al. reference, p. 8, lines 9-10), the tunnel diode formed by layers 1418, 1420 serves to provide polarity matching between the emitter layer 1414 and the Ge substrate 1402.

In view of the foregoing, it is clear that layers 1412, 1414 in the bypass diode 1410 of the Ho et al. reference do not correspond to the claimed sequence of layers that form a support for a bypass diode, as recited in claim 47.

The Examiner also alleges (Office Action at p. 19) that the substrate 1402 in the Ho et al. reference corresponds to the claimed "top layer" of a top cell and that the tunnel diode layer 1420 corresponds to the claimed "bottom layer" of a bypass diode. Applicant disagrees because a person of ordinary skill in the art would not consider the Ge substrate 1402 as the "top layer of the top cell." Indeed, as explained below, the Examiner's position is contrary to the ordinary use of the terminology in the art, including its use in the pending application and in the Ho et al. reference itself.

It is well known in the art that a "top" layer is labeled as such with reference to a substrate. For example, FIG. 6 of the present application shows a "top solar cell 608" (¶ 54) formed over a Ge substrate 602. Indeed, even the Ho et al. reference discloses that layers 1422, 1424 "form the conventional *top* cell" (p. 8, line 12). Therefore, a person of ordinary skill in the art would not regard the Ge substrate 1402, on which the solar cells are formed, as the "top layer of the top cell" as recited in pending claim 47.

In addition, pending claim 47 recites that the sequence of semiconductor layers which forms the sequence of cells in the first region is "laterally spaced apart and laterally separated" from the sequence of layers in the second region. However, FIG. 14B of the Ho *et al.* reference clearly illustrates that the substrate 1402 – which the Examiner alleges corresponds to the claimed "top layer of the top cell" – is formed as a *contiguous* layer extending from the

photovoltaic portions of the solar cell to the region in which the bypass diode 1410 is formed. Therefore, the substrate 1402 cannot correspond to the claimed "top layer of the top cell."

(ii) Claim 47 is patentable over JP 9-64397 (Fujioka)

As explained below, the Fujioka reference does not disclose a "sequence of layers of semiconductor material" that is "laterally spaced apart and laterally separated" and that forms "a support" for an integral bypass diode as recited in pending claim 47.

The Fujioka reference discloses variations of a solar cell device that includes a solar battery element (101, 201, 301) connected to a diode component (102, 202, 302), both of which include semiconductor layers on a substrate (103, 203, 303) (*see* FIGS. 1-3).

The Examiner alleges (*see* Office action mailed March 7, 2006, p. 10) that the layers 107D/108D, in diode component 102, and the layers 107/108, in solar battery element 101, correspond to the claimed "sequence of layers of semiconductor material" that is "laterally spaced apart and laterally separated" as recited in pending claim 47. That is incorrect.

The Fujioka reference discloses that layers 107 and 107D correspond to transparent electrodes and that the layers 208 and 208D correspond to current collection electrodes (*see* ¶ 33, 34). There is no disclosure in the Fujioka reference that the transparent electrodes 107/107D or current collection electrodes 108/108D are formed of semiconductor material. Indeed, one of ordinary skill in the art would presume that an electrode would instead be formed of a conducting material such as metal. Therefore, the Fujioka reference fails to disclose a "sequence of layers of *semiconductor* material" that is "laterally spaced apart and laterally separated" as recited in pending claim 47.

However, even if the layers 107D and 108D were formed of semiconductor material (which they are not), these layers do not form "a support" for an integral bypass diode as further recited by claim 47. Instead, FIG. 1 of the Fujioka reference clearly shows that the layers 107D and 108D are formed *above* i-type layer 105D and n(p)-type layer 104D of the diode component 102. Accordingly, there is no disclosure in the Fujioka reference of a sequence of layers of semiconductor material that form "a support" for a bypass diode.

The Examiner alleges (*see* Office Action, p. 10) that the layer 104D of diode component 102 corresponds to the claimed "bottom layer" of a bypass diode and that the layer 104A corresponds to the claimed "top layer of the top cell." That interpretation is incorrect.

As discussed above with respect to the Ho et al. reference, it is well known in the art that a "top" layer is labeled as such with reference to a substrate. It is also well known in the art that the "top" side of a solar cell is the side of the cell that receives light. However, FIGS 1 and 2 of the Fujioka reference show that layer 104A is formed at the *bottom* of the solar battery element 101 between conductive substrate 203 and i-type layer 105A. Likewise, layer 104D is formed *above* i-type layer 105D of the bypass diode component (*see* ¶ 38, FIGS. 1, 2). Furthermore, the Fujioka reference discloses, in reference to the diode element 302 of FIG. 3, that the element is "formed on the reverse (or *bottom*) side of...conductive substrate 301" (*see* ¶ 47) and that the diode element can "also be formed on both the *top* and bottom surfaces [of the conductive substrate]" (*see* ¶ 49). Accordingly, it is clear from the Fujioka reference that the terms "top" and "bottom" correspond to a particular and specific orientation. Therefore, a person skilled in the art would not consider the layer n(p)-type layer 104A of the solar battery element as the "top layer of the top cell" or the n(p)-type layer 104D as a "bottom layer" of a bypass diode.

In view of the foregoing remarks, the rejection of claim 47 under § 102(b) should be reversed.

(E) <u>The Rejection of Claim 69 Under 35 U.S.C. § 102(b) Should Be Reversed</u>

As explained by the MPEP (§ 2131), a claim is anticipated under 35 U.S.C. § 102(b) "only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." As discussed below, that is simply not the case here.

Among other things, claim 69 recites a solar cell semiconductor device that includes a bypass diode having "p-type, i-type, <u>and</u> n-type layers."

The Examiner alleges (*see* Office Action mailed March 6, 2007, p. 10, lines 6-8) that the Fujioka reference discloses a bypass diode (202) that includes p-type, i-type and n-type layers (205A, 204B and 207D) as recited in pending claim 69. Applicant respectfully disagrees.

There is no disclosure in the Fujioka reference that a bypass diode includes p-type, i-type, and n-type layers. Instead, the Fujioka reference discloses that each bypass diode component shown in FIGS. 1-3 only includes an "independent i-n or i-p junction" (*see* i-type layers 105A, 205A, 305A and n or p-type layers 104B, 204B, 304B as disclosed in ¶ 38, 41, 43, 46 and 48). The layers 107D, 207D and 307D formed above the i-n or i-p junctions are transparent electric conduction films (*see* ¶ 41, 44, 46) and do not correspond to any of the claimed p-type, i-type and n-type layers. The Examiner apparently reads the claim as if it recited a bypass diode having "p-type, i-type, *or* n-type layers." That clearly is not what the claim recites. Moreover, the Fujioka reference itself distinguishes the use of i-p or i-n junctions from p-i-n and n-i-p structures (¶ 38).

In view of the foregoing remarks, the rejection of claim 69 under § 102(b) should be reversed.

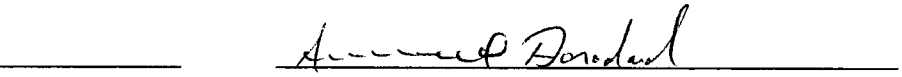
Summary

Applicant requests that all rejections of claims 37, 47 and 69 be reversed and that the claims be allowed.

The fee for the appeal brief is being paid concurrently herewith on the Electronic Filing System (EFS) by way of Deposit Account authorization. Please apply any other charges or credits to Deposit Account No. 06-1050.

Respectfully submitted,

Date: 5/31/07



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Appendix of Claims

37. An integrated semiconductor structure comprising:

a multijunction solar cell structure having at least first and second subcells; and

a bypass device integral to a subcell for passing current when the solar cell is shadowed and having p-type, i-type and n-type layers;

wherein the bypass device and the subcell have an identical sequence of semiconductor layers where each layer in the bypass device has substantially the same composition and thickness as the corresponding layer in the subcell and form an integral semiconductor body.

47. A solar cell semiconductor device comprising:

a semiconductor body having a sequence of layers of semiconductor material including a first region in which the sequence of layers of semiconductor material forms a sequence of cells of a multijunction solar cell with the top layer of the top cell having a first polarity; and

a second region in which the sequence of layers is laterally spaced apart and laterally separated from said first region and in which the sequence of layers forms a support for an integral bypass diode to protect said sequence of cells against reverse biasing at less than breakdown voltage, the bottom layer of the bypass diode having said first polarity

wherein the first region and the second region have an identical sequence of layers where each layer in the first region has substantially the same composition and thickness as the corresponding layer in the second region and form an integral semiconductor body.

69. A solar cell semiconductor device comprising:

a substrate;

a first sequence of layers of semiconductor material deposited on said substrate, including a first region in which the sequence of layers of semiconductor material forms at least one cell of a multijunction solar cell where the top layer of the top cell has a first polarity;

a second region including said first sequence of layers, and a second sequence of layers that forms a bypass diode to protect said at least one cell against reverse biasing at less than breakdown voltage where the bottom layer of the bypass diode has the same polarity as said first polarity of said top cell;

a metal layer deposited on a portion of said substrate and over at least a portion of said second region for electrically shorting the first sequence of layers of said second region and to electrically connect to said bypass diode in said second region; and

wherein the first region and the second region have an identical sequence of semiconductor layers where each layer in the second region has substantially the same composition and thickness as the corresponding layer in the first region and form an integral semiconductor body and wherein said bypass diode includes p-type, i-type, and n-type layers.

Evidence Appendix

In a previous reply (June 27, 2006), Applicant submitted a copy of a Declaration under 37 C.F.R. section 1.132. A copy of the Declaration is attached.

Related Proceedings Appendix

The present application is a continuation of U.S. Application No. 10/280,593, which is a continuation-in-part of U.S. Application No. 09/999,598.

An appeal to the Board of Appeals has been filed in connection with U.S. Application No. 10/723,456, which is continuation of U.S. Application No. 09/999,598.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Appl. No.	:	10/773,343	Confirmation No.: 6467
Applicant	:	Paul R. Sharps, *et al.*	
Filed	:	February 6, 2004	
TC/A.U.	:	1753	
Examiner	:	Diamond, Alan D.	

DECLARATION UNDER 37 C.F.R. § 1.132

I, Paul R. Sharps, declare that:

1. I am a resident of Albuquerque, New Mexico, and am an inventor in the above identified patent application.

2. As the Examiner notes, and may be deduced from the Figures and the specification, the composition and thickness of the layers of the triple junction solar cell according to the present invention are intended to be uniform over the surface of the wafer. Thus, the layers of the bypass diode and the layers of the adjacent solar cell are intended to have "the same" composition and thickness.

3. However, as is known to those skilled in the art, the actual deposition of III-V compound semiconductor layers over the surface of a substrate is a complex chemical process, and the "ideal" uniformity of a resulting wafer with precisely "the same" or identical composition and thickness of the layers at every point on the surface is a practical impossibility.

4. Although one may colloquially or loosely refer to the layers as having "the same" composition and thickness, in reality, the nature of the deposition process inherently results in small variations both in composition and in thickness of each layer over the surface of the wafer.

5. It is my experience that variations of two to three percent in composition and in thickness of a compound semiconductor layer over the surface of the wafer are quite normal and in fact are well within manufacturing specifications for actual commercial products.

6. Since the citation by the Examiner of the JP '397 reference has made it necessary to expressly refer to the composition and thickness of the layers in both the solar cell portion and the bypass diode portion of the semiconductor structure of the present invention, consideration must be given as to the most appropriate manner of expressing the fact that the layers are intended ideally to be "the same," unlike those in the JP '397 reference, while still describing and covering the actual processed compound semiconductor structures on wafers of the present invention. As noted above, neither the composition nor the thickness of deposited compound semiconductor layers are exactly "the same" or identical over the entire surface of the wafer.

7. The Remarks to the Amendment submitted by Applicant on November 7, 2005 noted that in the application as filed, figures 3-5 and the text describing those figures (from page 5, line 27 to page 8, line 4) describes how the bypass diode is constructed by etching a sequence

of epitaxially deposited layers forming a single or "integral" semiconductor structure so that the remaining layers after etching in one region form a bypass diode, and the remaining layers in the other region after etching form a multijunction solar cell, both regions being in a single semiconductor structure. Therefore, inherent as a result of the manufacturing process is the fact that the layers of the bypass diode have substantially the same composition and thickness because the bypass device and the subcell were formed from the same layers before etching, and the thickness of the remaining layers is not changed by the etching.

8. Therefore, out of an abundance of caution and in the interest of technical accuracy, rather than using the absolute expression "the same" in the claims, the undersigned submits that the phrase "substantially the same" is more accurate and is supported by the specification as would be understood by those skilled in the art reading a description of the fabrication process described from page 5, line 27 through page 8, line 4 of the application as filed.

9. I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believe to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code.

Signed in Albuquerque, New Mexico this 17th day of May 2006.

Paul R. Sharps

Paul R. Sharps